Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A system for transferring a signal to a channel, comprising:

a storage unit dedicated to the channel for storing source identification information of a plurality of predetermined sources, the source identification information indicating an order of priority of the plurality of predetermined sources for access to the channel;

a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the storage unit, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information; and

a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel,

wherein the storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

2. (Original) The system of claim 1, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

3. (Original) The system of claim 1, wherein the storage unit is a register.

4. (Previously Presented) The system of claim 1, wherein the storage unit stores the source identification information for the plurality of predetermined sources in order of priority of the sources for access to the channel.

5. (Cancelled)

6. (Original) The system of claim 1, wherein the storage unit sequentially stores the source identification information according to priority from the most significant bits to the least significant bits of the storage unit.

7. (Original) The system of claim 1, wherein the storage unit sequentially stores the source identification information according to priority from the least significant bits to the most significant bits of the storage unit.

8. (Original) The system of claim 1, wherein the circuit checks the outputs of the selection circuits in a predetermined sequence.

9. (Original) The system of claim 8, wherein the circuit sequentially checks the outputs of the selection circuits.

10. (Previously Presented) The system of claim 8, wherein the sequence is determined by an order in which the source identification information of the plurality of predetermined sources is stored in the storage unit.

11. (Previously Presented) The system of claim 1, wherein the circuit checks the outputs of the selection circuits in order of priority of the plurality of predetermined sources for forwarding input signals to the channel.

12. (Previously Presented) The system of claim 1, wherein the system includes a plurality of channels, input signals from the plurality of predetermined sources being able to be forwarded to the plurality of channels.

13. (Original) The system of claim 12, further comprising a plurality of storage units associated respectively with the plurality of channels.

14. (Previously Presented) The system of claim 13, wherein each of the storage units stores source identification information for a plurality of predetermined sources that are

able to forward input signals onto the channel associated with the storage unit.

15. (Original) The system of claim 1, wherein the selection circuits are multiplexers.

16. (Original) The system of claim 15, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

17. (Previously Presented) The system of claim 16, wherein the multiplexers are ordered according to priorities of the plurality of predetermined sources for forwarding input signals to the channel.

18. (Previously Presented) The system of claim 1, wherein the plurality of predetermined sources are applied to inputs of the selection circuits according to a predetermined order.

19. (Previously Presented) The system of claim 18, wherein the predetermined order depends on priority of the plurality of predetermined sources for access to the channel.

20. (Previously Presented) The system of claim 18, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the plurality of predetermined sources based on priority of the plurality of predetermined sources for access to the channel.

21. (Original) The system of claim 1, further comprising a channel unit associated with the channel for processing information related to the channel.

22. (Original) The system of claim 21, wherein the storage unit is part of the channel unit.

23. (Currently Amended) A system for transferring signals to channels, comprising;
a plurality of storage units, each storage unit being dedicated to one of the

channels, and each storage unit being adapted to store source identification information indicating an order of priority of a plurality of predetermined sources for access to the channel;

for each of the plurality of channels, a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the plurality of storage units, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel,

wherein each storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

24. (Original) The system of claim 23, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

25. (Previously Presented) The system of claim 23, wherein one or more of the plurality of predetermined sources are allocated to one or more of the channels.

26. (Previously Presented) The system of claim 25, wherein the allocation of the plurality of predetermined sources to the channels is controllable by controlling storage of source identification information in the storage units.

27. (Original) The system of claim 23, wherein the storage units are registers.

28. (Previously Presented) The system of claim 23, wherein each of the storage units stores its source identification information for the plurality of predetermined sources in order of priority of the plurality of predetermined sources for access to the associated channel.

29. (Original) The system of claim 23, wherein the selection circuits are

multiplexers.

30. (Original) The system of claim 29, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

31. (Previously Presented) The system of claim 29, wherein the multiplexers are ordered according to priorities of the plurality of predetermined sources for forwarding input signals to the channels.

32. (Previously Presented) The system of claim 23, wherein the plurality of predetermined sources are applied to inputs of the selection circuits according to a predetermined order.

33. (Previously Presented) The system of claim 32, wherein the predetermined order depends on priority of the plurality of predetermined sources for access to the channels.

34. (Previously Presented) The system of claim 32, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the plurality of predetermined sources based on priority of the plurality of predetermined sources for access to the channels.

35. (Original) The system of claim 23, further comprising a plurality of channel units associated respectively with the plurality of channels for processing information related to the channels.

36. (Original) The system of claim 35, wherein each of the storage units is part of one of the channel units.

37. (Currently Amended) A direct memory access (DMA) controller for controlling transfer of signals from predetermined input sources to output devices, a plurality of channels being connected to the output devices, the DMA controller comprising:

a plurality of storage units, each storage unit being dedicated to one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the predetermined sources for access to the channel;

for each of the plurality of channels, a plurality of selection circuits for receiving input signals from at least one of the predetermined sources and the source identification information of the predetermined sources from the plurality of storage units, each of the selection circuits selecting one of the plurality of input in response to the source identification information; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel,

wherein each storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

38. (Original) The DMA controller of claim 37, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

39. (Previously Presented) The DMA controller of claim 37, wherein one or more of the predetermined sources are allocated to one or more of the channels.

40. (Previously Presented) The DMA controller of claim 37, wherein the allocation of the predetermined sources to the channels is controllable by controlling storage of source identification information in the storage units.

41. (Original) The DMA controller of claim 37, wherein the storage units are registers.

42. (Previously Presented) The DMA controller of claim 37, wherein each of the storage units stores its source identification information for the predetermined sources in order of priority of the predetermined sources for access to the associated channel.

43. (Original) The DMA controller of claim 37, wherein the selection circuits are

multiplexers.

44. (Original) The DMA controller of claim 43, wherein the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit.

45. (Previously Presented) The DMA controller of claim 43, wherein the multiplexers are ordered according to priorities of the predetermined sources for forwarding input signals to the channels.

46. (Previously Presented) The DMA controller of claim 37, wherein the predetermined sources are applied to inputs of the selection circuits according to a predetermined order.

47. (Previously Presented) The DMA controller of claim 46, wherein the predetermined order depends on priority of the predetermined sources for access to the channels.

48. (Previously Presented) The DMA controller of claim 46, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the predetermined sources based on priority of the predetermined sources for access to the channels.

49. (Original) The DMA controller of claim 37, further comprising a plurality of channel units associated respectively with the plurality of channels for processing information related to the channels.

50. (Original) The DMA controller of claim 40, wherein each of the storage units is part of one of the channel units.

51. (Currently Amended) A method for transferring a signal to a channel, comprising:

storing source identification information for a plurality of predetermined sources in a storage unit, the source identification information indicating an order of priority of the plurality of predetermined sources for access to the channel;

providing a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information;

with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel,

wherein the storage unit stores the source identification information for a highest-priority source in the most significant bits of the storage unit.

52. (Original) The method of claim 51, wherein each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit.

53. (Original) The method of claim 51, wherein the storage unit is a register.

54. (Previously Presented) The method of claim 51, wherein the storage unit stores the source identification information for the plurality of predetermined sources in order of priority of the plurality of predetermined sources for access to the channel.

55. (Cancelled)

56. (Original) The method of claim 51, wherein the storage unit sequentially stores the source identification information according to priority from the most significant bits to the least significant bits of the storage unit.

57. (Original) The method of claim 51, wherein the storage unit sequentially stores the source identification information according to priority from the least significant bits to the most significant bits of the storage unit.

58. (Original) The method of claim 51, wherein the circuit checks the outputs of the selection circuits in a predetermined sequence.

59. (Original) The method of claim 58, wherein the circuit sequentially checks the outputs of the selection circuits.

60. (Previously Presented) The method of claim 58, wherein the sequence is determined by an order in which the source identification information of the plurality of predetermined sources is stored in the storage unit.

61. (Previously Presented) The method of claim 51, wherein the checking circuit checks the outputs of the selection circuits in order of priority of the plurality of predetermined sources for forwarding input signals to the channel.

62. (Previously Presented) The method of claim 51, wherein the communication system includes a plurality of channels, input signals from the plurality of predetermined sources being able to be forwarded to the plurality of channels.

63. (Original) The method of claim 62, further comprising providing a plurality of storage units associated respectively with the plurality of channels.

64. (Previously Presented) The method of claim 63, wherein each of the storage units stores source identification information for a plurality of predetermined sources that are able to forward input signals onto the channel associated with the storage unit.

65. (Original) The method of claim 51, wherein the selection circuits are multiplexers.

66. (Original) The method of claim 65, wherein the multiplexers are ordered according to the sequence of the source identification information stored n the storage unit.

67. (Previously Presented) The method of claim 65, wherein the multiplexers are ordered according to priorities of the plurality of predetermined sources for forwarding input signals to the channel.

68. (Previously Presented) The method of claim 51, wherein the plurality of predetermined sources are applied to inputs of the selection circuits according to a predetermined order.

69. (Previously Presented) The method of claim 68, wherein the predetermined order depends on priority of the plurality of predetermined sources for access to the channel.

70. (Previously Presented) The method of claim 68, wherein the source identification information is generated according to the predetermined order such that the selection circuits select the plurality of predetermined sources based on priority of the plurality of predetermined sources for access to the channel.

71. (Original) The method of claim 51, further comprising a channel unit associated with the channel for processing information related to the channel.

72. (Original) The method of claim 71, wherein the storage unit is part of the channel unit.